

An Alternative Procedure for Implementing the Desegmentation Method

P. C. SHARMA, MEMBER, IEEE, AND K. C. GUPTA, SENIOR MEMBER, IEEE

Abstract—A new procedure for implementing the desegmentation method for analyzing two-dimensional microwave circuits is proposed. In certain situations, the condition for which has been brought out in this paper, the proposed procedure leads to more efficient evaluation of impedance matrices than the procedure known earlier. The computational efforts in the two procedures are compared.

I. INTRODUCTION

THE GREEN'S FUNCTION approach for analysis of 2-4 microwave circuits was proposed a decade ago [1]. The applicability of this approach has been extended to circuits of more general shapes (than those for which Green's functions are available) by the segmentation [2]–[4] and the desegmentation [5] methods. For example, the circuit configuration of Fig. 1(a) can be analyzed employing the segmentation method by considering this circuit pattern as having been obtained by combining rectangular and isosceles triangular segments, as illustrated in Fig. 1(b). The computational effort in the method of analysis is largely governed by the number of interconnected ports [4]. For example, if the truncation of the rectangular segment is large, such as along the dotted lines shown in Fig. 1(a), the number of interconnected ports (as shown in Fig. 1(c)) would be smaller in the case when the truncation is small, as shown in (Fig. 1(b)). The analysis for the circuit in Fig. 1(c) will, therefore, require a smaller amount of computational effort as compared to that needed for the circuit of Fig. 1(b).

The circuit configuration of Fig. 1(a) can, alternatively, be analyzed by considering the circuit as obtained by removal of two isosceles triangular segments from a rectangular segment (Fig. 1(d)). The Z -parameters of the α -circuit are obtained from those of β - and γ -segments. This alternative approach has been named as the desegmentation method [5]. The interconnections between various segments in Fig. 1(d) would be smaller as compared to those in the case of Fig. 1(b).

There are situations where the segmentation method cannot be applied, but the desegmentation method can still be used. One such circuit configuration is shown in Fig.

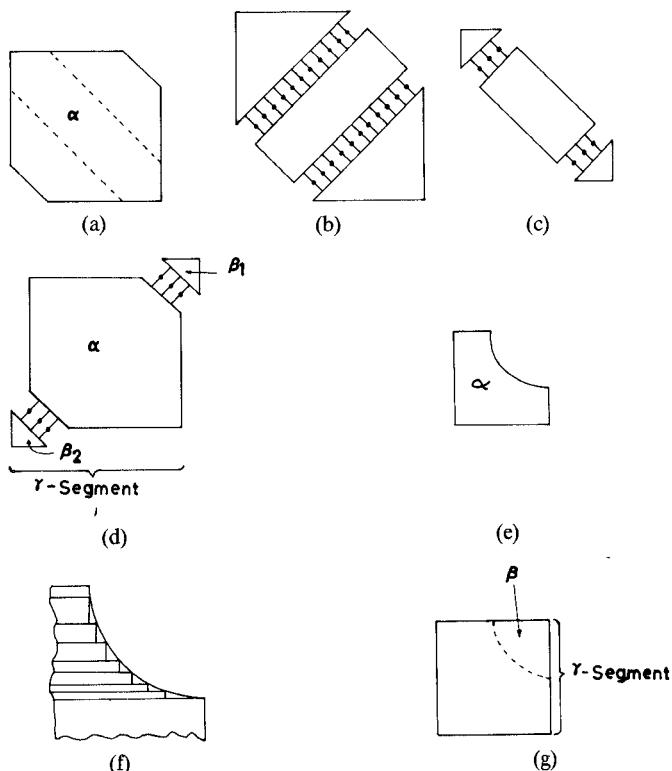


Fig. 1. (a) α -circuit to be analyzed, (b) its segmentation, (c) segmentation of α when truncated along dotted lines, (d) desegmentation applied to the α -circuit, (e) another circuit α to be analyzed, (f) segmentation applied to the α -circuit shown in (e), and (g) its desegmentation.

1(e). If the analysis of this circuit is attempted by employing the segmentation method, the curved boundary is to be approximated by a piecewise linear boundary. The number of triangular and rectangular segments in such a situation becomes too large, as illustrated in an enlarged view of the region in Fig. 1(f). Moreover, for some of these triangles, the Green's functions may not be available. The desegmentation method [5] can still be used to analyze the circuit of Fig. 1(e) by considering it as having been obtained by the removal of a sector β from a rectangle γ as shown in Fig. 1(g). Detailed discussions on segmentation and desegmentation methods have already been reported in the literature [2]–[5].

An alternative approach for implementation of the desegmentation method is proposed in this paper. The previous procedure [5] is reviewed briefly in Section II and the new procedure is discussed in Section IV. Since the validity

Manuscript received July 6, 1982; revised July 5, 1983.

P. C. Sharma is with the Department of Electronics and Communication Engineering, S.G.S. Institute of Technology and Science, Indore 452003, India.

K. C. Gupta is with the Electromagnetics Laboratory, Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309.

of the segmentation method has already been demonstrated [5]–[8], an example is given in Section V to verify the new procedure by comparing the results with those obtained by previous procedure [5].

II. THE PREVIOUS PROCEDURE

The α -circuit of Fig. 2(a) is considered for explaining the procedure known earlier [5] and the procedure proposed in this paper. The Z-parameters at ports P_1 and C_1 are needed. When a rectangular segment (β) is added to the α -segment, the resulting combination is another rectangular segment γ (Fig. 2(b)). The α - and β -segments are interconnected by a discrete number of ports, named c -ports on α -segment and d -ports on β -segment. Thus the number of c -ports ($=C$) always equals the number of d -ports ($=D$). The specified c -port (C_1 in Fig. 2(a)) forms one of the c -ports. The number of interconnected ports are large enough so that discrete interconnections between the α - and β -segments are approximate to the continuous connection at the interface between these segments. The Z-matrices for β - and γ -segments are evaluated employing the Green's function for a rectangle [1] and are expressed as

$$\tilde{Z}_\beta = \begin{bmatrix} \tilde{Z}_{dd} & \tilde{Z}_{dq} \\ \tilde{Z}_{qd} & \tilde{Z}_{qq\beta} \end{bmatrix} \quad \tilde{Z}_\gamma = \begin{bmatrix} \tilde{Z}_{pp\gamma} & \tilde{Z}_{pq} \\ \tilde{Z}_{qp} & \tilde{Z}_{qq\gamma} \end{bmatrix}. \quad (1)$$

Referring to the nomenclature of the ports as shown in Fig. 2(a) and (b), it has been shown that when the number of q -ports ($=Q$) and of d -ports ($=D$) are equal, the impedance matrix for the α -segment can be expressed in terms of the Z-matrices of β - and α -segments as

$$\tilde{Z}_\alpha = \begin{bmatrix} \tilde{Z}_{pp\alpha} & \tilde{Z}_{pc} \\ \tilde{Z}_{cp} & \tilde{Z}_{cc} \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{pp\gamma} - \tilde{Z}_{pq}\tilde{Z}'_{qp} & -\tilde{Z}_{pq}\tilde{Z}'_{qd} \\ -\tilde{Z}_{dq}\tilde{Z}'_{qp} & -\tilde{Z}_{dd} - \tilde{Z}_{dq}\tilde{Z}'_{qd} \end{bmatrix} \quad (2)$$

where

$$\tilde{Z}'_{qp} = [\tilde{Z}_{qq\gamma} - \tilde{Z}_{qq\beta}]^{-1} \tilde{Z}_{qp}$$

and

$$\tilde{Z}'_{qd} = [\tilde{Z}_{qq\gamma} - \tilde{Z}_{qq\beta}]^{-1} \tilde{Z}_{qd}.$$

It has been shown earlier [5] that, when Z-parameters at only p -ports on the α -segment are required, (2) reduces to

$$\tilde{Z}_\alpha = \tilde{Z}_{pp\alpha} = \tilde{Z}_{pp\gamma} - \tilde{Z}_{pq}[\tilde{Z}_{qq\gamma} - \tilde{Z}_{qq\beta}]^{-1} \tilde{Z}_{qp}. \quad (3)$$

The preceding equation does not involve the submatrices \tilde{Z}_{dd} , \tilde{Z}_{dq} , and \tilde{Z}_{qd} . Only $\tilde{Z}_{qq\beta}$ and \tilde{Z}_γ are required for evaluating $\tilde{Z}_{pp\alpha}$.

It is proposed in this paper that, in addition to the Z-parameters at p -ports, those at c -ports can also be evaluated by employing (3). The modified procedure requires renaming the various ports on the α -segment as discussed in Section IV. In order for the computational efforts in the two procedures (in using (2) and (3)) to be

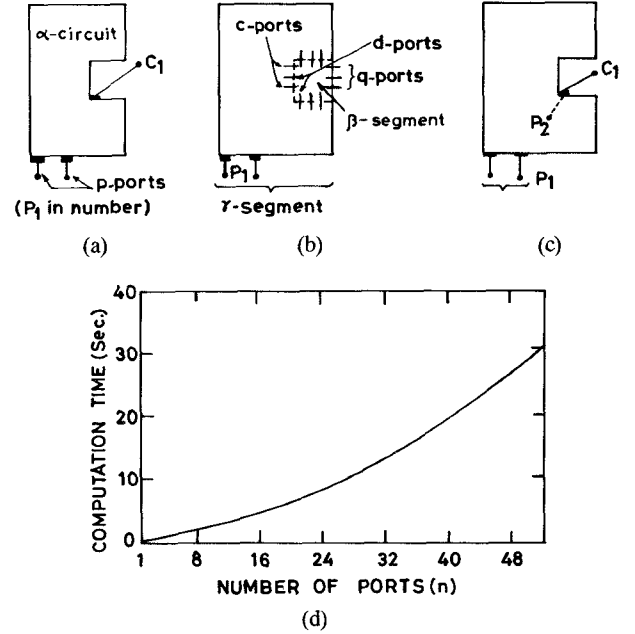


Fig. 2. (a) A circuit to be analyzed. (b) The circuits' desegmentation according to the previous procedure. (c) A modified port nomenclature for implementing the new desegmentation procedure. (d) Computational time needed as a function of the number of ports.

compared, a brief discussion of the computational effort requirement in the previous procedure is included in Section III.

III. COMPUTATIONAL EFFORT IN THE PREVIOUS PROCEDURE

The circuit shown in Fig. 2(a) is used for illustration. Equation (2) is used to evaluate the Z-parameters at specified p - and c -ports (such as P_1 number of p -ports and the port C_1 in Fig. 2(a)). As discussed in the preceding Section, this requires additional c -ports to be incorporated at the interface between α - and β -segments so as to satisfy $Q = D$ ($=C$). In this case, all the submatrices of \tilde{Z}_β and \tilde{Z}_γ are needed. As seen from (1), the orders of the matrices \tilde{Z}_β and \tilde{Z}_γ , to be evaluated from the Green's function [1], are $(D + Q)$ by $(D + Q)$, i.e., $2Q$ by $2Q$ since $D = Q$, and $(P_1 + Q)$ by $(P_1 + Q)$, respectively.

It may be mentioned here that, in implementing the desegmentation method, the most time-consuming computational step is the evaluation of the impedance matrices for β - and γ -segments. For any regularly shaped n -port segment, evaluation of an n by n Z-matrix requires the evaluation of integrals (at n -ports) of the terms occurring in the expression for the Green's function. Evaluation of these integrals is the most time-consuming computational step when compared to other mathematical operations involved. Actual variation of the computation time with n , the number of ports, for a regular rectangular segment is shown in Fig. 2(d). Computations were carried out on a DEC-1090 computer system. As a first-order approximation, the computational effort may be taken as proportional to the number of ports n . If $E(\beta)$ is the computational effort needed in evaluating the integrals at one of the

TABLE I
ORDERS OF THE Z-MATRICES AND COMPUTATIONAL EFFORTS IN
IMPLEMENTING THE DESEGMENTATION METHOD

| | Procedure I (Section 2) | Procedure II (Section 4) |
|---|---|--|
| 1. Orders of \tilde{Z}_p and $\tilde{Z}_{qp\beta}$ respectively | $2Q \times 2Q$ | $Q \times Q$ |
| 2. Order of \tilde{Z}_γ | $(P_1+Q) \times (P_1+Q)$ | $(P_1+P_2+Q) \times (P_1+P_2+Q)$ |
| 3. Computational effort | $E_1 = 2Q E(\beta) + (P_1+Q) E(\gamma)$ | $E_2 = Q E(\beta) + (P_1+P_2+Q) E(\gamma)$ |

ports of the β -segment, and $E(\gamma)$ is the corresponding effort for the γ -segment, the total computational effort in evaluating \tilde{Z}_β and \tilde{Z}_γ is

$$E_1 = 2QE(\beta) + (P_1 + Q)E(\gamma). \quad (4)$$

IV. MODIFIED PROCEDURE

In this method, all the original ports of the α -segment (even when they are located at the interface between α - and β -segments) are treated as unconnected p -ports. For interconnection to β -segment, additional ports (called c -ports) can be located at the same place as each one of the p -ports along the common boundary. As shown in Fig. 2(c), P_2 is the unconnected original port of α -segment, whereas C_1 is a c -port added for connecting it to the corresponding D_1 port on the β -segment. Since the Z -matrix is required for only p -ports of the α -segment, (3) can be used. The matrices \tilde{Z}_γ and $\tilde{Z}_\beta (= \tilde{Z}_{qp\beta})$ that are needed in (3) are of orders $(P_1 + P_2 + Q)$ by $(P_1 + P_2 + Q)$, and Q by Q , respectively. The computational effort, to the same approximation as in (4), in evaluating these matrices, is given by

$$E_2 = QE(\beta) + (P_1 + P_2 + Q)E(\gamma). \quad (5)$$

A brief summary of the above discussion is given in Table I. The computational effort in (4) and (5) are equal if $QE(\beta) = P_2E(\gamma)$. When the β - and γ -segments are similar (i.e., both are rectangular or the same type of triangles, etc.), one obtains $E(\beta) = E(\gamma)$. In such a situation, the computational efforts E_1 and E_2 (in (4) and (5), respectively) are equal if $Q = P_2$. In other words, if the number of specified P_2 -ports on the common boundary (Fig. 1(a), (b), (c)) is equal to the number of q -ports ($= Q$), the computational efforts in both the procedures discussed above are equal. But, in practice, the number of P_2 -ports ($= P_2$) is much less than the number of q -ports required for convergence, and the modified procedure turns out to be more efficient.

In general, depending upon the number of P_2 -ports, one may choose to employ one of the two procedures. Reduction in the size of the matrices leads to savings in storage requirements and computational time.

V. ILLUSTRATIVE EXAMPLE

The α -circuit considered for illustration is shown in Fig. 3(a) (inset). The impedance parameters for ports P_1 and P_2 , of widths 2.5 and 0.4 mm, respectively, are to be evaluated.

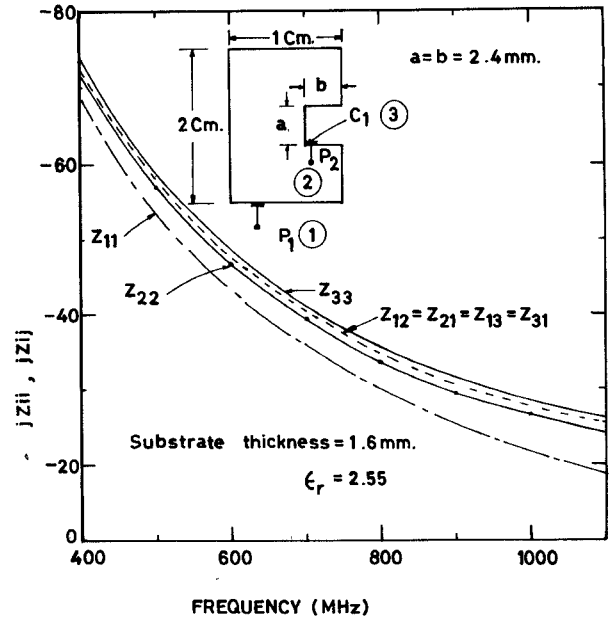


Fig. 3. Impedance parameters for a sample circuit obtained by the two desegmentation procedures.

The β - and γ -segments are rectangular patterns as shown in Fig. 2(b).

The number of q -ports needed for convergence of the impedance parameters is 18 at the highest frequency (1.1 GHz) of interest. Correspondingly, there are 18 d -ports (on the β -segment) and, therefore, 18 c -ports (on the α -segment) at the interface between β - and α -segments, and (2) and (3) could be used. The port C_1 , in Fig. 2(c), is one of the 18 c -ports. The location and width of the port C_1 are identical to those of the port P_2 (Fig. 2(c)). The ports P_1 , P_2 , and C_1 are numbered as 1, 2, and 3. The circuit has been analyzed by using the procedure of Section II as well as that proposed in Section IV. The parameters evaluated are Z_{11} , $Z_{13} (= Z_{31})$, and Z_{33} by the first method (Section II), and Z_{11} , $Z_{12} (= Z_{21})$, and Z_{22} by the second method (Section IV). It may be noted that the parameters Z_{11} in either cases must be identical. Also, the parameters $Z_{13} (= Z_{31})$ and $Z_{12} (= Z_{21})$ should be equal since the locations and widths of the ports P_2 and C_1 are identical. For the same reason, the parameters Z_{33} and Z_{22} should be equal to each other.

Fig. 3 illustrates the variations of these parameters as functions of frequency. The values of $Z_{12} (= Z_{21})$ and $Z_{13} (= Z_{31})$, as obtained by the two procedures discussed in Sections II and IV, respectively, are so close to each other that separate curves could not be plotted. Values of Z_{11} as obtained by the two procedures also exhibit similar behavior (Fig. 3). Z_{22} and Z_{33} variations are also in reasonable agreement. Thus the results shown in Fig. 3 prove the validity of the procedure proposed in this paper.

Table II illustrates that the procedure proposed in this paper is computationally more efficient than the procedure given earlier. Although the computational effort (Table II) in evaluating a Z -matrix of order 18×18 is not half of that in evaluating a 36×36 matrix from Green's function, the first-order approximation (that computational time is pro-

TABLE II
ORDERS OF Z-MATRICES AND COMPUTATIONAL EFFORT IN
EVALUATING Z_α FOR THE CIRCUIT SHOWN IN FIG. 3

| | Procedure of Section 2 | Procedure of Section 4 |
|--|---------------------------|---------------------------|
| 1. Order of : | | |
| i) Z_p and Z_{qp} respectively | 36×36 | 18×18 |
| ii) Z_y | 19×19 | 20×20 |
| 2. Computational effort (seconds) in evaluating | | |
| i) Z_p and Z_{qp} respectively | 16.36 | 6.01 |
| ii) Z_y | 6.28 | 6.37 |
| iii) Z_α from Eqs. (2) and (3) respectively | 5.18 | 0.66 |
| 3. Total computational effort (in seconds) on DEO-1090 computer system | 27.82 | 13.04 |

portional to the number of ports) used in deriving (4) and (5) may still be used for the purpose of comparing the computational efficiency of one procedure with the other.

VI. CONCLUSIONS

A new algorithm for analyzing two-dimensional circuits by the desegmentation method has been proposed. The validity of the procedure is illustrated by an example. For the typical example chosen, the proposed procedure is shown to be more efficient than the procedure known earlier. An approximate criterion is developed for estimating the efficiency of one procedure over the other.

REFERENCES

- [1] T. Okoshi and T. Miyoshi, "The planar circuit—An approach to microwave integrated circuitry," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 245–252, Apr. 1972.
- [2] T. Okoshi and T. Takeuchi, "Analysis of planar circuits by segmentation method," *Electron. Commun. Japan*, vol. 58-B, no. 8, pp. 71–79, 1975.
- [3] T. Okoshi, T. Uehara, and T. Takeuchi, "The segmentation method—An approach to the analysis of planar microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 662–668, Oct. 1976.
- [4] R. Chadha and K. C. Gupta, "Segmentation method using impedance matrices for analysis of planar microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 71–74, Jan. 1981.
- [5] P. C. Sharma and K. C. Gupta, "Desegmentation method for analysis of two-dimensional microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 1094–1098, Oct. 1981.
- [6] K. C. Gupta and P. C. Sharma, "Segmentation and desegmentation techniques for analysis of planar microstrip antennas," in *1981 IEEE AP-S Int. Symp. Dig.*, pp. 19–22.
- [7] P. C. Sharma and K. C. Gupta, "Optimized design of single feed circularly polarized microstrip patch antennas," in *1982 IEEE AP-S Int. Symp. Dig.*, pp. 156–159.

- [8] R. Chadha and K. C. Gupta, "Compensation of discontinuities in planar transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 2151–2156, Dec. 1982.



P. C. Sharma (S'79–M'82) was born at Bhensola, Ujjain, India, on August 1, 1947. He received the B.E. and M.E. degrees in electrical engineering in 1969 and 1972, respectively, from the Shri Govindram Seksaria Institute of Technology and Science Indore, University of Indore, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1982.

He worked with the Military College of Telecommunication Engineering, Mhow, India, during 1971. In 1972, he joined S.G.S. Institute of Technology and Science in the Department of Electrical Engineering, where he is presently employed as a Reader in the Department of Electronics and Telecommunication Engineering. He has over ten papers to his credit in various transactions and conferences. His fields of interest are systems engineering, networks, electromagnetics, and microstrip antennas.

Dr. Sharma is a member of the Institution of Engineers, and a member of the Institution of Instrumentation Scientists and Technologists, both in India, as well as a member of the Indian Society for Technical Education.



K. C. Gupta (M'62–SM'74) was born in 1940. He received the B.E. and M.E. degrees in electrical communication engineering from the Indian Institute of Science, Bangalore, India, in 1961 and 1962, respectively, and the Ph.D. degree from the Birla Institute of Technology and Science, Pilani, India, in 1969.

He worked at Punjab Engineering College, Chandigarh, India, from 1964 to 1965, the Central Electronics Engineering Research Institute, Pilani, India, from 1965 to 1968, and Birla Institute of Technology from 1968 to 1969. Since 1969, he has been with the Indian Institute of Technology, Kanpur, India, and has been a Professor of Electrical Engineering since 1975. On leave from the Indian Institute of Technology, he was a Visiting Professor at the University of Waterloo, Canada, from 1975 to 1976, Ecole Polytechnique Federale de Lausanne, Switzerland, in 1976, Technical University of Denmark from 1976 to 1977, and Eidgenossische Technische Hochschule, Zurich, Switzerland, in 1979. From 1971 to 1979, he was Coordinator for the Phased Array Radar Group of Advanced Centre for Electronic Systems at the Indian Institute of Technology. He is presently a Visiting Professor at the University of Colorado, Boulder. He has published four books: *Microwave Integrated Circuits* (Wiley Eastern and Halsted Press, 1974), *Microstrip Lines and Slotlines* (Artech House, 1979), *Microwaves* (Wiley Eastern, 1979, Halsted Press, 1980), and *Computer-Aided Design of Microwave Circuits* (Artech House, 1981). He has published over 80 research papers and holds one patent in the microwave area.

Dr. Gupta is a fellow of the Institution of Electronics and Telecommunication Engineers in India.